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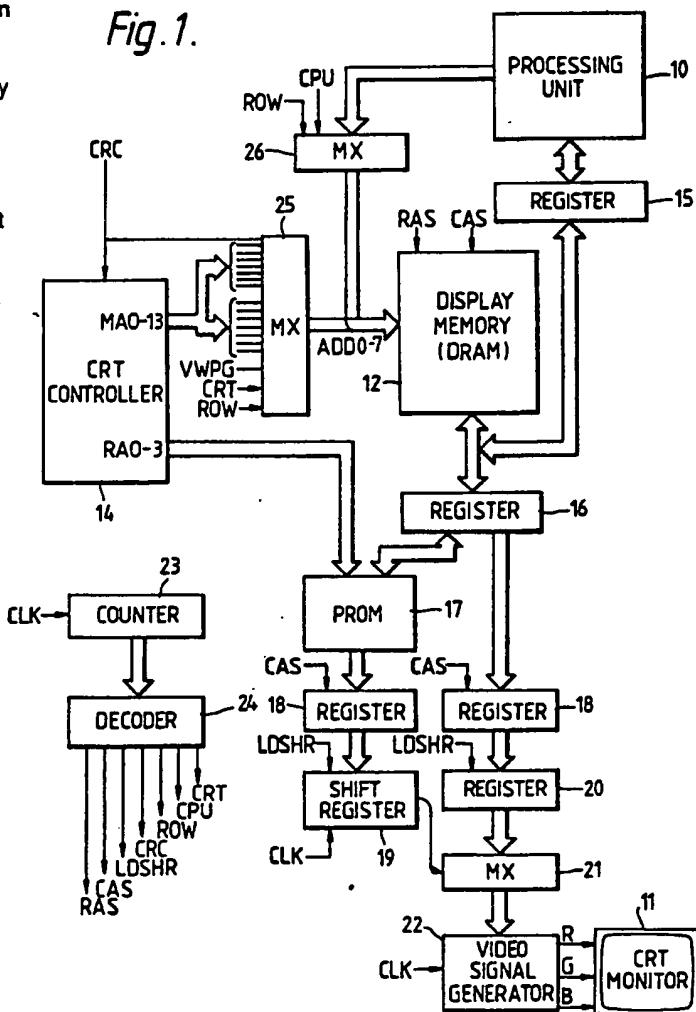
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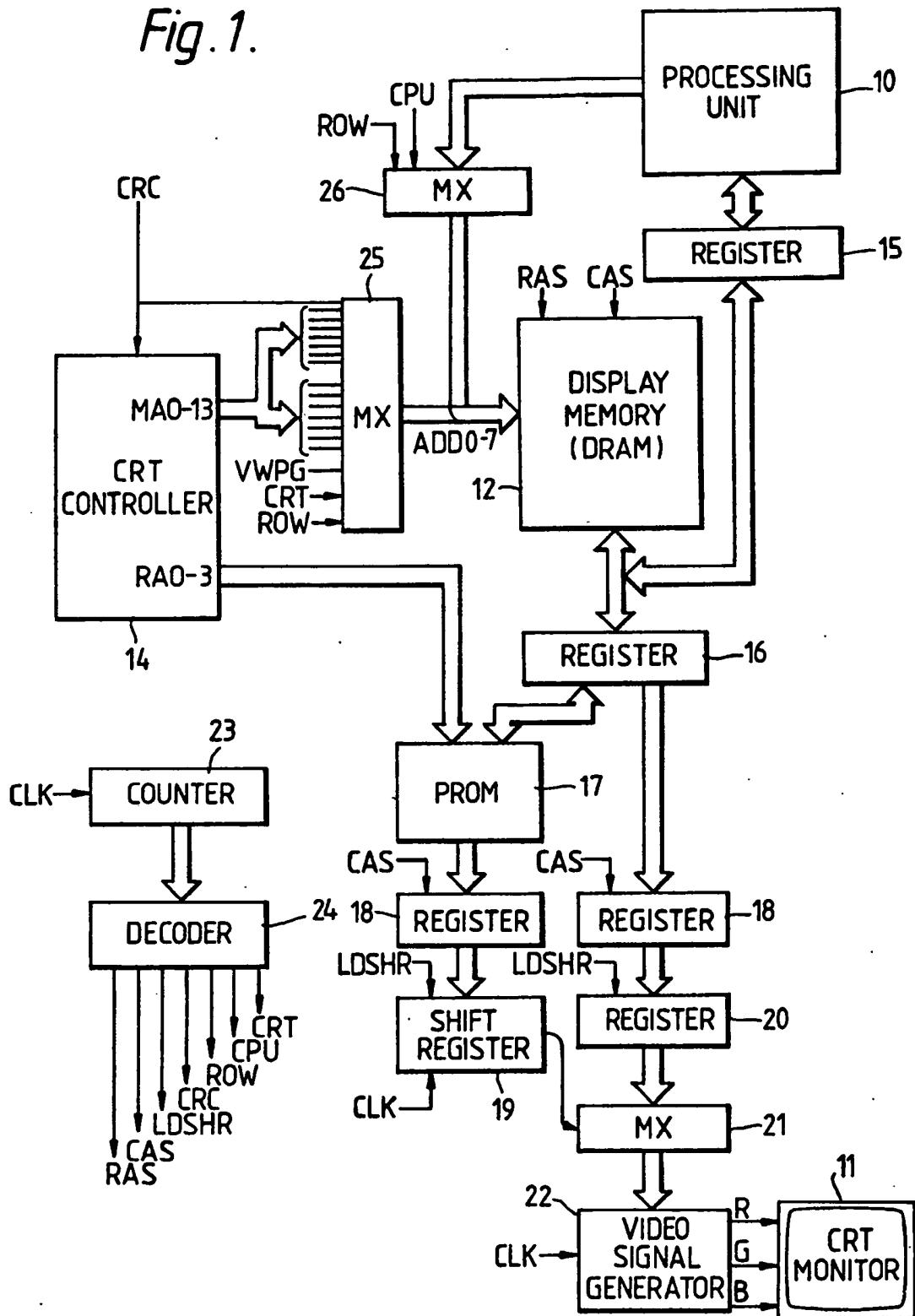
(54) Data display memory addressing system

(57) Data is held in a display memory 12 and then read out sequentially to produce the display by apparatus including a controller device 14, e.g. a conventional CRT controller chip, which generates a sequence of addresses. The controller is driven by a clock signal, which causes the controller to increment its address at each clock beat. The actual address for the display memory has the clock signal as its least significant bit, the remaining bits being provided by the address from the controller. In this way, two locations in the display memory are accessed for each address from the controller, so that the rate of access of the memory is doubled.



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Fig. 1.



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Fig. 2 CLK processor $\overline{\text{RAS}}$ video accesses

The diagram illustrates the timing of various signals for a processor. The CLK signal is a continuous square wave. The RAS signal is asserted (low) during the first half of each clock cycle. The CAS signal is asserted during the second half of each clock cycle. The REG.16 and REG.18 signals are both labeled 'rubbish' and show a sequence of values: REG.16 starts at 3, goes to 0, then 1, then 2, then 3 again; REG.18 starts at 2, goes to 3, then 0, then 1, then 2 again. The LDSHR signal is asserted during the second half of the clock cycle when REG.16 is 0. The shift signal is asserted during the second half of the clock cycle when REG.18 is 0. The req signal is asserted during the second half of the clock cycle when REG.16 is 3.

Fig. 3

The diagram illustrates the timing sequence for memory access. The **CLK** signal is a continuous square wave. The **RAS** signal is asserted (low) during the first half of the first clock cycle. The **CAS** signal is asserted (low) during the second half of the first clock cycle. The **video accesses** signal is asserted (high) during the second half of the first clock cycle. The **0**, **1**, **2**, and **3** signals are asserted (high) sequentially during the second, third, fourth, and fifth halves of the first clock cycle, respectively. The **CRC** signal is asserted (high) during the second half of the second clock cycle.

DATA DISPLAY APPARATUSBackground to the invention

15 This invention relates to data display apparatus. More specifically, the invention is concerned with display apparatus in which data to be displayed is stored in a memory, and then read out in a predetermined sequence to generate the necessary signals for producing the display.

20 Controller devices for generating the required sequence of addresses for reading out data from a display memory are well known, and are available as standard integrated circuit chips. In use, the controller is driven by an input clock signal, which steps the controller through a sequence of states so as to produce a sequence of address signal outputs, as well as other control signals, 25 such as blanking and synchronisation signals.

30 Clearly, such a controller has a certain maximum speed of operation, determined by the maximum clock rate at which it will operate. This limits the rate at which accesses can be made to the display memory and hence limits the amount of information which can be displayed at any given time.

35 The object of the present invention is to overcome this limitation, by providing a way of addressing the display memory at a faster rate than the maximum allowable clock rate of the controller.

Summary of the invention

According to the invention there is provided data display apparatus comprising
(a) a display memory,

(b) means for generating a clock signal,
(c) a display controller device for producing a
sequence of address signals when clocked by said
clock signal, and
5 (d) means for addressing the display memory with an
address consisting of a combination of the clock
signal and the address signal from the controller.
10 It can be seen that, since the clock signal
changes value in each clock period, the display address has
two different values in each clock period. Thus, the rate
at which the display memory is addressed is doubled.

Brief description of the drawings

15 One embodiment of the invention will now be
described by way of example with reference to the
accompanying drawings.

Figure 1 shows a data processing system including
data display apparatus.

20 Figures 2 and 3 are timing diagrams illustrating
the operation of the apparatus.

Description of an embodiment of the invention

Referring to Figure 1, the data processing system
comprises a data processing unit 10. Data from the
25 processing unit can be displayed on a video display device
which, in this example, consists of a conventional cathode
ray tube (CRT) monitor 11.

The data to be displayed is stored in a display
memory 12. This comprises a dynamic random-access memory
30 (DRAM) containing 64K individually addressable 16-bit word
locations. The memory 12 is a conventional row/column
organised memory, having internal row and column address
registers. The row address register is loaded with an
8-bit row address from an input address path ADD0-7, at the
35 falling edge of a row address strobe signal RAS.

Similarly, the column address register is loaded with an
8-bit column address from ADD0-7 at the falling edge of a
column address strobe signal CAS. The contents of the row
and column address registers together select one word in
the memory for reading or writing.

5 The addresses on the address path ADD0-7 are derived from the processing unit 10, in the case of processor accesses, or from a conventional CRT controller 14, in the case of video accesses. For example, the controller 14 may be a Fujitsu MB 89321 single-chip CMOS device.

10 Each 16-bit word in the memory 12 consists of two 8-bit bytes. The first byte represents the identity of a character to be displayed, while the second byte represents one or more attributes of that character. In this particular example, the second byte consists of two 4-bit colour codes. The first of these codes represents the 15 foreground colour (i.e. the colour of the character itself) while the second code represents the background colour (i.e. the colour surrounding the character).

20 The currently addressed location of the memory 12 can be accessed, by way of a 16-bit register 15, by the processing unit 10, allowing the processing unit to read the contents of the location or to write new data into that location.

25 The output of the currently addressed location of the memory is also clocked into a 16-bit register 16 at the next rising edge of the CAS signal.

30 The first byte of the register 16, representing the character code, is connected to the address input of a character look-up table, consisting of a programmable read-only memory (PROM) 17. The address input of the PROM 17 also receives a character line address RA0-3 from the CRT controller 14, indicating which raster line of the character is currently being scanned. The data output of the character PROM 17 is an 8-bit word, indicating display values for the eight successive picture elements (pixels) 35 making up the portion of the selected character in the current scan line.

 The output of the character PROM 17, and the second byte of the register 16, are clocked into a sixteen-bit register 18 at the next again rising edge of the CAS signal.

5 The first byte of the register 18 (containing the data from the character PROM 17) is clocked into an eight-bit shift register 19 by means of a shift register load control signal LDSHR. At the same time, the second byte of the register 18 (representing the character attributes) is gated into an eight-bit register 20.

10 The contents of the shift register 19 are then shifted out, one bit at a time, by means of a clock signal CLK, at the desired pixel rate of the display. In this particular example, the clock CLK has a frequency of 20 MHz. The output bit from the shift register 19 controls a multiplexer 21 which selects either the foreground or the 15 background colour code from the register 20.

20 The selected 4-bit colour code from the multiplexer 21 is fed to a video signal generator circuit 22, which converts the code into one of sixteen pre-programmed colours, by generating the appropriate red, green and blue (RGB) video signals for the CRT monitor 11.

25 The CRT controller 14 is programmable to produce a sequence of 14-bit memory addresses MA0-13. The controller 14 is driven by a clock signal CRC such that, at each falling edge of CRC, a new memory address MA0-13 is produced, except during blanking periods.

30 The address path ADD0-7 of the DRAM 12 is connected to the output of a multiplexer 25. This can be enabled by a signal CRT which permits the CRT controller 14 to access the DRAM. When enabled, the multiplexer 25 35 alternatively selects two eight-bit inputs, according to the value of a control signal ROW. When ROW is low, the multiplexer selects a column address, the least significant bit of which consists of the clock signal CRC and the other seven bits of which consist of the signals MA 0-2, MA 7-10 from the controller 14. Conversely, when ROW is high, the multiplexer selects a row address, the most significant bit of which consists of a control signal VWPG which selects between two possible pages for display, and the remaining seven bits of which consist of the signals MA 3-6, MA 11-13 from the controller.

5 It can be seen that, since the column address supplied to the DRAM via the multiplexer 25 has the clock signal CRC as its least significant bit, the column address has two different values in each period of CRC. Hence, two different locations in the DRAM are addressed for each value of the address MA 0-13 from the controller.

10 The address path ADD0-7 of the DRAM 12 is also connected to the output of a multiplexer 26. This can be enabled by a signal CPU, which permits the processing unit 10 to access the DRAM. When enabled, the multiplexer 26 alternately selects either a row address or a column address from the processing unit 10, according to the value 15 of the signal ROW.

20 The pixel rate clock signal CLK drives a 5-bit counter 23, which defines a 32-beat cycle of operation for the apparatus. The contents of this counter are decoded by a decoder circuit 24 to produce various control signals during the cycle, including the signals RAS, CAS, LDSHR, 25 CRC, ROW, CPU and CRT mentioned above.

25 Referring now to Figure 2, this is a timing diagram showing one of these cycles of operation. In each cycle, one processor access and four video accesses (0-3) are made to the display memory DRAM 12.

30 At the first falling edge of RAS in each cycle, a row address from the processing unit 10 is strobed into the memory 12. Then, at the falling edge of CAS, a column address from the processing unit is strobed into the memory. The addressed location of the memory can then be accessed by the processing unit.

35 At the next falling edge of RAS, a row address from the CRT controller 14 is strobed into the memory 12. Then, at the next four falling edges of CAS, four successive column addresses are strobed from the controller 14. Thus, four successive locations in the memory are accessed, all these locations having the same row address but having different column addresses. These are the four video accesses (0-3).

It can be seen that the data from these four video

accesses is skewed, in the sense that the accesses all take place towards one end of the cycle, and are therefore not equally spaced through the cycle.

5 The data read from the memory in each video access is clocked into the register 16 at the first rising edge of CAS following the access. Then, at the next rising edge of CAS, the data is clocked into the register 18. In the interval between the clocking of the two registers 16, 18, the first byte of the data is converted by the character 10 look-up table 17. It should be noted that the data appearing at the output of the memory during the processor access is also clocked through the registers 16, 18. However, this data is not intended to be displayed, and hence is regarded as "rubbish" when it passes through the 15 registers 16, 18.

15 Figure 2 also shows the signal LDSHR which clocks the output of the register 18 into the shift register 19 and the register 20. As can be seen, this signal LDSHR occurs at equally spaced intervals of eight beats of the 20 clock CLK, four times in each cycle. The signal LDSHR is aligned with the data in register 18 in such a manner that it samples the data from the four video accesses, but ignores the "rubbish" data.

25 In summary, it can be seen that the signal CAS divides each cycle into five sub-cycles, in which the data from the five memory accesses (one processor access and four video accesses) are respectively loaded into the register 18. The signal LDSHR divides each cycle into four equal sub-cycles, in which the data from the four video 30 accesses is read out of the register 18. The video data is thus de-skewed, and the "rubbish" data is discarded.

35 Referring now to Figure 3, this again shows the signals CLK, RAS and CAS, and shows the clock signal CRC which drives the CRT controller. At each falling edge of CRC, the CRT controller increments its memory address MA0-13, as illustrated by the least significant bit MA0 of this address.

It can be seen that, for each value of the address MA 0-13, the clock signal CRC has two values: first low and then high. Hence, two locations of the display memory are accessed for each value of the address MA 0-13; in other 5 words, the display memory is addressed at twice the rate of operation of the CRT controller. Moreover, the potential address range of the CRT controller is doubled by the extra address bit CRC.

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CLAIMS:-

1. Data display apparatus comprising
 - (a) a display memory,
 - (b) means for generating a clock signal,
 - 5 (c) a display controller device for producing a sequence of address signals when clocked by said clock signal, and
 - (d) means for addressing the display memory with an address consisting of a combination of the clock signal and the address signal from the controller.
- 10 2. Apparatus according to Claim 1 wherein the clock signal forms the least significant bit of the address for the display memory.
- 15 3. Apparatus according to Claim 1 or 2 having a cycle of operation, wherein, in each cycle of operation one processor access and a plurality n of video accesses can be made to the display memory.
- 20 4. Apparatus according to Claim 3 wherein said clock signal has $n/2$ periods during each of said cycles of operation, each of said periods being aligned with a pair of said video accesses.
- 25 5. Data display apparatus substantially as hereinbefore described with reference to the accompanying drawings.